Raspberry Pi Compute Module 4 SODIMM

Colophon

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IMPORTANT

The Raspberry Pi Compute Module 4 SODIMM (CM4S) is intended for specific industrial customers migrating from Compute Module 3 or Compute Module 3+ and is not for general sale. For new customers who are designing products, we recommend using Raspberry Pi Compute Module 4.

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1. Introduction

1.1. Introduction

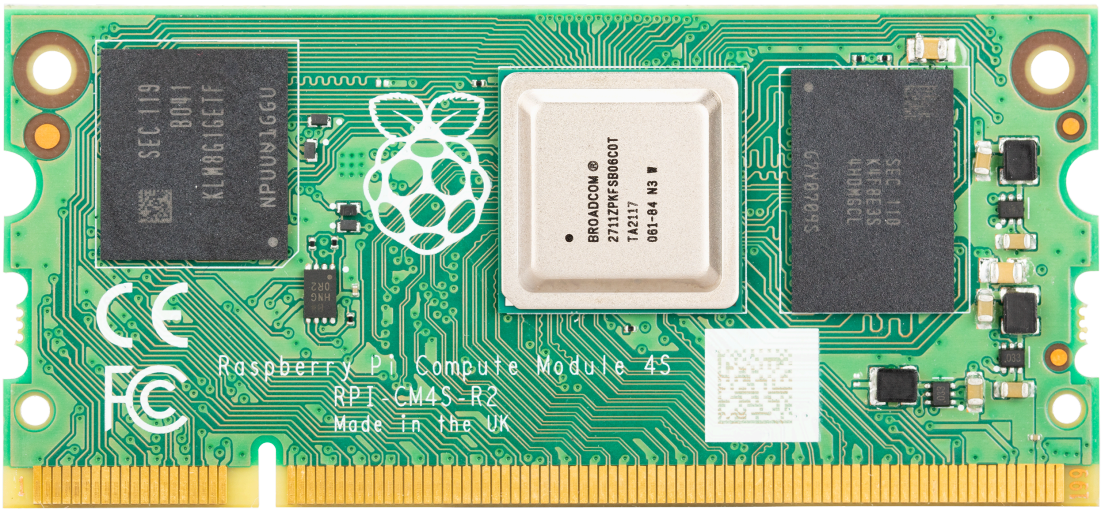

Figure 1. The Raspberry Pi Compute Module 4 SODIMM (CM4S).

The Raspberry Pi Compute Module 4 SODIMM (CM4S) is a System on Module (SoM) containing processor, memory, eMMC Flash, and supporting power circuitry. These modules allow a designer to leverage the Raspberry Pi hardware and software stack in their own custom systems and form factors. In addition, these modules have extra GPIO over and above what is available on the Raspberry Pi boards, opening up more options for the designer.

The design of the CM4S is loosely based on the Raspberry Pi 4 Model B, and for cost-sensitive applications it can be supplied without the eMMC fitted; this version is called the Raspberry Pi Compute Module 4 SODIMM Lite (CM4SLite).

The CM4S is in the same form factor as the older Raspberry Pi Compute 3 and 3+ modules, which are mechanically compatible with DDR2-SODIMM.

NOTE

The CM4S SoC has a slightly increased z-height over the Raspberry Pi Compute Module 3.

NOTE

Unless otherwise stated, for this document CM4S also refers to CM4SLite.

1.2. Features

Key features of the CM4S are as follows:

- Broadcom BCM2711, quad core Cortex-A72 (ARM v8) 64-bit SoC @ 1.5GHz
- DDR2-SODIMM-mechanically-compatible form factor
- H.265 (HEVC) (upto 4Kp60 decode), H.264 (upto 1080p60 decode, 1080p30 encode)
- OpenGL ES 3.0 graphics
- 1GB LPDDR4-3200 SDRAM with ECC (see Appendix B)

- Options for 0GB **(CM4SLite)**, 8GB, 16GB, or 32GB eMMC flash memory (see Appendix B)
    - Peak eMMC bandwidth 100MBps (four times faster than previous Compute Modules)
- 1 × USB 2.0 port (high speed)
- 46 × GPIO supporting either 1.8V or 3.3V signalling and peripheral options:
    - Up to 6 × UART
    - Up to 6 × I2C
    - Up to 6 × SPI
    - 1 × SDIO interface
    - 1 × DPI (parallel RGB display)
    - 1 × PCM
    - Up to 2× PWM channels
    - Up to 3× GPCLK outputs
- 1 × HDMI 2.0 ports (up to 4Kp60 supported)
- MIPI DSI:
    - 1 × 2-lane MIPI DSI display port
    - 1 × 4-lane MIPI DSI display port
- MIPI CSI-2:
    - 1 × 2-lane MIPI CSI camera port
    - 1 × 4-lane MIPI CSI camera port
- 1 × SDIO 2.0 **(CM4SLite)**

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2. Interfaces

2.1. USB 2.0 (high speed)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Ω differential pair. The length of the P/N signals should ideally be matched to better than 0.15mm.

TIP

The firmware disables the USB interface by default to save power. In recent versions of Raspberry Pi OS (Bullseye) it is automatically enabled by the `otg_mode=1` setting in the config.txt file. If you are using a different OS, or an older version of Raspberry Pi OS, you will need to add this to config.txt to enable the USB interface.

NOTE

The port is capable of being used as a true USB On-The-Go (OTG) port. While there is no official documentation, some users have had success making this work. The `USB_OTGID` pin is used to select between USB host and device that is typically wired to the ID pin of a Micro USB connector. To use this functionality it must be enabled in the OS. If using either as a fixed slave or fixed master, please tie the `USB_OTGID` pin to ground.

2.2. GPIO

There are 46 pins available for general purpose I/O (GPIO); 28 of them correspond to the GPIO pins on the Raspberry Pi 4 Model B 40-pin header. The 46 pins have access to internal peripherals: SMI, DPI, I2C, PWM, SPI, and UART. The BCM2711 ARM peripherals book describes these features in detail, along with the multiplexing options available. The drive strength and slew rate should ideally be set as low as possible to reduce any EMC issues.

The BCM2711 GPIO bank0 is powered by `GPIO0-27_VDD`, and GPIO bank1 is powered by `GPIO28-45_VDD`. These can either be connected to +1.8V for 1.8V signalling GPIO, or +3.3V for 3.3V signalling. You should keep the load on each GPIO bank to below 50mA in total. `GPIO0-27_VDD` and `GPIO28-45_VDD` must be powered for the CM4S to start up correctly.

NOTE

If GPIO0 or GPIO1 are not used for HAT id purposes, then to prevent the firmware from checking to see if there is a HAT EEPROM available, add `force_eeprom_read=0` and `disable_poe_fan=1` to the config.txt file.

2.2.1. Alternative function assignments

Up to six alternative functions are available. The BCM2711 ARM peripherals book describes these features in detail. The table below gives a quick overview.

Table 1. GPIO pins alternative function assignment

GPIO	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO0	High	SDA0	SA5	PCLK	SPI3_CE0_N	TXD2	SDA6
GPIO1	High	SCL0	SA4	DE	SPI3_MISO	RXD2	SCL6
GPIO2	High	SDA1	SA3	LCD_VSYNC	SPI3_MOSI	CTS2	SDA3
GPIO3	High	SCL1	SA2	LCD_HSYNC	SPI3_SCLK	RTS2	SCL3
GPIO4	High	GPCLK0	SA1	DPI_D0	SPI4_CE0_N	TXD3	SDA3
GPIO5	High	GPCLK1	SA0	DPI_D1	SPI4_MISO	RXD3	SCL3
GPIO6	High	GPCLK2	SOE_N / SE	DPI_D2	SPI4_MOSI	CTS3	SDA4
GPIO7	High	SPI0_CE1_N	SWE_N / SRW_N	DPI_D3	SPI4_SCLK	RTS3	SCL4

GPIO8	High	SPI0_CE0_N	SD0	DPI_D4	BSCSL / CE_N	TXD4	SDA4
GPIO9	Low	SPI0_MISO	SD1	DPI_D5	BSCSL / MISO	RXD4	SCL4
GPIO10	Low	SPI0_MOSI	SD2	DPI_D6	BSCSL SDA / MOSI	CTS4	SDA5
GPIO11	Low	SPI0_SCLK	SD3	DPI_D7	BSCSL SCL / SCLK	RTS4	SCL5
GPIO12	Low	PWM0_0	SD4	DPI_D8	SPI5_CE0_N	TXD5	SDA5
GPIO13	Low	PWM0_1	SD5	DPI_D9	SPI5_MISO	RXD5	SCL5
GPIO14	Low	TXD0	SD6	DPI_D10	SPI5_MOSI	CTS5	TXD1
GPIO15	Low	RXD0	SD7	DPI_D11	SPI5_SCLK	RTS5	RXD1
GPIO16	Low	<reserved>	SD8	DPI_D12	CTS0	SPI1_CE2_N	CTS1
GPIO17	Low	<reserved>	SD9	DPI_D13	RTS0	SPI1_CE1_N	RTS1
GPIO18	Low	PCM_CLK	SD10	DPI_D14	SPI6_CE0_N	SPI1_CE0_N	PWM0_0
GPIO19	Low	PCM_FS	SD11	DPI_D15	SPI6_MISO	SPI1_MISO	PWM0_1
GPIO20	Low	PCM_DIN	SD12	DPI_D16	SPI6_MOSI	SPI1_MOSI	GPCLK0
GPIO21	Low	PCM_DOUT	SD13	DPI_D17	SPI6_SCLK	SPI1_SCLK	GPCLK1
GPIO22	Low	SD0_CLK	SD14	DPI_D18	SD1_CLK	ARM_TRST	SDA6
GPIO23	Low	SD0_CMD	SD15	DPI_D19	SD1_CMD	ARM_RTCK	SCL6
GPIO24	Low	SD0_DAT0	SD16	DPI_D20	SD1_DAT0	ARM_TDO	SPI3_CE1_N
GPIO25	Low	SD0_DAT1	SD17	DPI_D21	SD1_DAT1	ARM_TCK	SPI4_CE1_N
GPIO26	Low	SD0_DAT2	<reserved>	DPI_D22	SD1_DAT2	ARM_TDI	SPI5_CE1_N
GPIO27	Low	SD0_DAT3	<reserved>	DPI_D23	SD1_DAT3	ARM_TMS	SPI6_CE1_N
GPIO28	-	SDA0	SA5	PCM_CLK	<reserved>	MII_A_RX_ERR	RGMII_MDIO
GPIO29	-	SCL0	SA4	PCM_FS	<reserved>	MII_A_TX_ERR	RGMII_MDC
GPIO30	Low	<reserved>	SA3	PCM_DIN	CTS0	MII_A_CRS	CTS1
GPIO31	Low	<reserved>	SA2	PCM_DOUT	RTS0	MII_A_COL	RTS1
GPIO32	Low	GPCLK0	SA1	<reserved>	TXD0	SD_CARD_PRES	TXD1
GPIO33	Low	<reserved>	SA0	<reserved>	RXD0	SD_CARD_WRPROT	RXD1
GPIO34	High	GPCLK0	SOE_N / SE	<reserved>	SD1_CLK	SD_CARD_LED	RGMII_IRQ
GPIO35	High	SPI0_CE1_N	SWE_N / SRW_N		SD1_CMD	RGMII_START_STOP	
GPIO36	High	SPI0_CE0_N	SD0	TXD0	SD1_DAT0	RGMII_RX_OK	MII_A_RX_ERR
GPIO37	Low	SPI0_MISO	SD1	RXD0	SD1_DAT1	RGMII_MDIO	MII_A_TX_ERR
GPIO38	Low	SPI0_MOSI	SD2	RTS0	SD1_DAT2	RGMII_MDC	MII_A_CRS
GPIO39	Low	SPI0_SCLK	SD3	CTS0	SD1_DAT3	RGMII_IRQ	MII_A_COL
GPIO40	Low	PWM1_0	SD4		SD1_DAT4	SPI0_MISO	TXD1
GPIO41	Low	PWM1_1	SD5	<reserved>	SD1_DAT5	SPI0_MOSI	RXD1

GPIO42	Low	GPCLK1	SD6	<reserved>	SD1_DAT6	SPI0_SCLK	RTS1
GPIO43	Low	GPCLK2	SD7	<reserved>	SD1_DAT7	SPI0_CE0_N	CTS1
GPIO44	-	GPCLK1	SDA0	SDA1	<reserved>	SPI0_CE1_N	SD_CARD_VOLT
GPIO45	-	PWM0_1	SCL0	SCL1	<reserved>	SPI0_CE2_N	SD_CARD_PWR0

Special function legend:

Table 2. GPIO pins alternative function legend

Name	Function
SDA0	BSC master 0 data line[a]
SCL0	BSC master 0 clock line
SDAx	BSC master 1,3,4,5,6 data line[b]
SCLx	BSC master 1,3,4,5,6 clock line
GPCLKx	General purpose clock 0,1,2
SPIx_CE2_N	SPI 0,3,4,5,6 chip select 2
SPIx_CE1_N	SPI 0,3,4,5,6 chip select 1
SPIx_CE0_N	SPI 0,3,4,5,6 chip select 0
SPIx_MISO	SPI 0,3,4,5,6 MISO
SPIx_MOSI	SPI 0,3,4,5,6 MOSI
SPIx_SCLK	SPI 0,3,4,5,6 serial clock
PWMx_0	PWM 0,1 channel 0
PWMx_1	PWM 0,1 channel 1
TXDx	UART 0,2,3,4,5 transmit data
RXDx	UART 0,2,3,4,5 receive data
CTSx	UART 0,2,3,4,5 clear to send
RTSx	UART 0,2,3,4,5 request to send
PCM_CLK	PCM clock
PCM_FS	PCM frame sync
PCM_DIN	PCM data in
PCM_DOUT	PCM data out
SAx	Secondary mem address bus
SOE_N / SE	Secondary mem controls
SWE_N / SRW_N	Secondary mem controls
SDx	Secondary mem data bus
BSCSL SDA / MOSI	BSC slave data, SPI slave MOSI

BSCSL SCL / SCLK	BSC slave clock, SPI slave clock
BSCSL - / MISO	BSC <not used>, SPI MISO
BSCSL - / CE_N	BSC <not used>, SPI CSn
SPI1_CE2_N	SPI 1 chip select 2 [c]
SPI1_CE1_N	SPI 1 chip select 1
SPI1_CE0_N	SPI 1 chip select 0
SPI1_MISO	SPI 1 MISO
SPI1_MOSI	SPI 1 MOSI
SPI1_SCLK	SPI 1 serial clock
TXD1	UART 1 transmit data
RXD1	UART 1 receive data
CTS1	UART 1 clear to send
RTS1	UART 1 request To send
ARM_TRST	ARM JTAG reset
ARM_RTCK	ARM JTAG return clock
ARM_TDO	ARM JTAG data out
ARM_TCK	ARM JTAG clock
ARM_TDI	ARM JTAG data in
ARM_TMS	ARM JTAG mode select
PCLK	Display parallel interface
DE	Display parallel interface
LCD_VSYNC	Display parallel interface
LCD_HSYNC	Display parallel interface
DPI_Dx	Display parallel interface

[a] The Broadcom serial control bus is a proprietary bus compliant with the Philips® I2C bus/interface.

[b] BSC master 2 & 7 are not user-accessible.

[c] SPI 2 is not user-accessible.

2.3. HDMI 2.0

The CM4S supports one HDMI 2.0 interface capable of driving 4K images.

HDMI signals should be routed as 100Ω differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm. Pairs don't typically need any extra matching, as they only have to be matched to 25mm.

CEC is also supported; an internal 27kΩ pullup resistor is included in the CM4S.

2.4. CSI-2 (MIPI serial camera)

The CM4S supports two camera ports: `CAM0` (2 lanes) and `CAM1` (4 lanes). CSI signals should be routed as 100Ω differential pairs. Each signal within a pair should ideally be matched to better than 0.15mm.

The documentation around the CSI interface can be found on the Raspberry Pi website, while Linux kernel drivers can be found on GitHub.

NOTE

The official Raspberry Pi firmware supports the OmniVision OV5647, Sony IMX219 and Sony IMX477 camera sensors. No security device is required on Compute Module devices in order to use these camera sensors.

2.5. DSI (MIPI serial display)

The CM4S supports two display ports: `DISP0` (2 lanes) and `DISP1` (4 lanes). Each lane supports a maximum data rate per lane of 1Gbps.

Although Linux kernel drivers are available, the DSI interface is not currently documented. Only DSI displays supported by the official Raspberry Pi firmware are supported. DSI signals should be routed as 100Ω differential pairs; each signal within a pair should ideally be matched to better than 0.15mm.

NOTE

While only official DSI displays are supported, other displays can be added using the parallel DPI interface which is available as a GPIO alternative function. The CM4S supports up to three displays of any type (HDMI, DSI, DPI) at any one time.

2.6. SDIO/eMMC (CM4SLite only)

The CM4SLite does not have on-board eMMC. The eMMC signals are available on the connector so that an external eMMC or SD card can be used.

The `SDX_VDD` signal is used to power the CM4SLite SDIO/eMMC interface and can therefore be used to set the SDIO voltage to either +3.3V or +1.8V.

2.7. Composite (TV out)

The TVDAC pin can be used to output composite video (PAL or NTSC). Please route this signal away from noise sources and use a 75Ω PCB trace.

NOTE

The TVDAC is powered from the VDAC supply, which must be a clean supply of 2.5-2.8V. It is recommended that users generate this supply from +3.3V using a low noise LDO. If the TVDAC output is not used, VDAC can be connected to +3.3V, but it must be powered even if the TV-out functionality is unused.

2.8. RUN

This pin when high signals that the CM4S has started. Driving this pin low resets the module. This should be done with caution; if files on a filesystem are open they will not be closed.

2.9. EMMC_DISABLE_N

This pin when low signals to the BCM2711 that boot should not occur from either an SD card or eMMC, forcing USB boot. This pin is internally pulled up to 3.3V via a 10kΩ resistor.

2.10. EMMC_EN_N_1V8

This pin is driven low to signal that the BCM2711 wishes to access the SD card or eMMC. Typically this is connected via a FET to the `EMMC_DISABLE_N` pin. If this pin is also connected to a LED, then any error that occurs during booting will flash an error pattern on this LED, which can be decoded using the look up table on the Raspberry Pi website.

2.11. EEPROM_nWP

It is recommended that final products connect this pin to ground to prevent end users changing the contents of the on-board EEPROM. See the Raspberry Pi 4 Model B documentation for instructions on the software settings required to support EEPROM write protection.

3. Electrical and mechanical

3.1. Mechanical

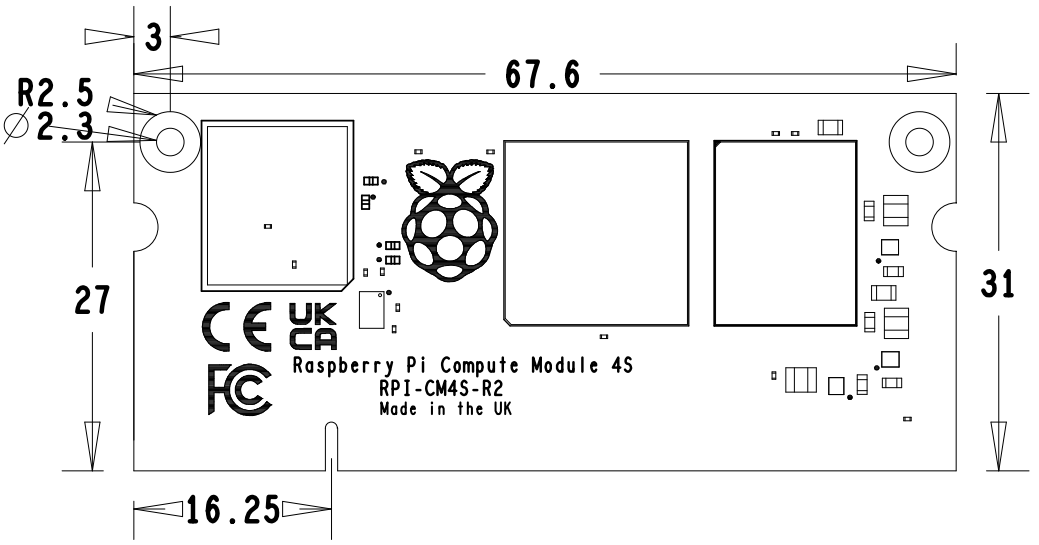
The CM4S modules conform to JEDEC MO-224 mechanical specification for 200-pin DDR2 (1.8V) SODIMM modules, so should work with the many DDR2 SODIMM sockets available on the market.

NOTE

The pinout of the CM4S is not the same as a DDR2 SODIMM module; they are **not** electrically compatible.

1. 2 × M1 mounting holes (inset 3mm from module edge).
2. PCB thickness 1mm ± 10%.
3. BCM2711 SoC height including solder balls 2.378 ± 0.11mm.
4. The maximum component height on the underside of the Compute Module is 1.2mm.
5. The maximum component height on the top side of the Compute Module is 2.5mm.

Figure 2. Mechanical specification of the Raspberry Pi Compute Module 4 SODIMM



NOTE

The location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however the maximum component heights and PCB thickness will be kept as specified.

A step file of the CM4S is available as part of the CM4S design data package. This is for guidance only and is subject to changes over time due to revisions.

3.2. Thermal

The CM4S dissipates less power than the Raspberry Pi 4 Model B. The CM4S also contains less metal in the PCB and fewer connectors, which means that it has less passive heat sinking than the Raspberry Pi 4 Model B. Despite it consumi-

ng less power, it may run warmer than the Raspberry Pi 4 Model B.

The BCM2711 will reduce the clock rate to try and keep its internal temperature below 85°C. So in high ambient temperatures it is possible that the clock will also be automatically throttled back. If the BCM2711 is unable to lower its internal clocks enough to bring the temperature down, its case temperature will rise above 85°C. It is important that any thermal solution chosen keeps the ambient temperature for the other silicon devices on the CM4S within the operating temperature range.

Operating temperature range: -20°C - +85°C non-condensing.

3.3. Electrical specification

WARNING

Stresses above those listed in Table 3 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{BAT}	Core SMPS Supply	-0.5	5.5	V
V_{3V3}	+3.3V Supply	-0.5	3.6	V
V_{DAC}	TV DAC Supply	-0.5	3.6	V
$V_{GPIOx\text{-}y\_VDD}$	GPIO Voltage	-0.5	3.6	V
V_{SDX_VDD}	SDIO Voltage	-0.5	3.6	V
V_{gpio}	GPIO Input voltage	-0.5	$V_{GPIOx\text{-}y\_VDD}$ + 0.5	V

Table 4. Operating ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{BAT}	Core SMPS Supply	2.5	5.25	V
V_{3V3}	+3.3V Supply	3.15	3.45	V
V_{DAC}	TV DAC Supply	2.37	3.45	V
$V_{GPIOx\text{-}y\_VDD}$	GPIO Voltage	1.71	3.45	V
V_{SDX_VDD}	SDIO Voltage	1.71	3.45	V

NOTE

$V_{GPIOx\text{-}y\_VDD}$ is the GPIO bank voltage (either `GPIO0-27_VDD` or `GPIO28-45_VDD`), each of which must be tied to either the 3.3V or the 1.8V rail of the CM4S.

Table 5. DC characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(gpio)}$	Input low voltage	$V_{GPIOx\text{-}y\_VDD}$ = 3.3V	0	-	0.8	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIOx\text{-}y\_VDD}$ = 3.3V	2.0	-	$V_{GPIOx\text{-}y\_VDD}$	V

$V_{IL(gpio)}$	Input low voltage	$V_{GPIOx\text{-}y\_VDD}$ = 1.8V	0	-	0.35	V
$V_{IH(gpio)}$	Input high voltage	$V_{GPIOx\text{-}y\_VDD}$ = 1.8V	0.65	-	$V_{GPIOx\text{-}y\_VDD}$	V
$I_{IL(gpio)}$	Input leakage current	-	-	-	10	µA
$V_{OL(gpio)}$	Output low voltage	-	-	-	0.4	V
$V_{OH(gpio)}$	Output high voltage	-	$V_{GPIOx\text{-}y\_VDD}$ - 0.4	-	-	V
$I_{O(gpio)}$	Output current	1mA	0.87	1.3	-	mA
$I_{O(gpio)}$	Output current	2mA	1.75	2.6	-	mA
$I_{O(gpio)}$	Output current	3mA	2.63	3.9	-	mA
$I_{O(gpio)}$	Output current	4mA **default**	3.5	5.3	-	mA
$I_{O(gpio)}$	Output current	5mA	4.39	6.6	-	mA
$I_{O(gpio)}$	Output current	6mA	5.27	7.9	-	mA
$I_{O(gpio)}$	Output current	7mA	6.15	9.2	-	mA
$I_{O(gpio)}$	Output current	8mA	7.02	10.5	-	mA
$R_{PU(gpio)}$	Pullup resistor	$V_{GPIOx\text{-}y\_VDD}$ = 3.3V	33	47	73	kΩ
$R_{PD(gpio)}$	Pulldown resistor	$V_{GPIOx\text{-}y\_VDD}$ = 3.3V	33	47	73	kΩ
$R_{PU(gpio)}$	Pullup resistor	$V_{GPIOx\text{-}y\_VDD}$ = 1.8V	18	47	73	kΩ
$R_{PD(gpio)}$	Pulldown resistor	$V_{GPIOx\text{-}y\_VDD}$ = 1.8V	18	47	73	kΩ

Refer to interface specifications (see Chapter 2) for electrical details of other interfaces.

Table 6. Power consumption

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
P_{idle}	Idle power		-	1.5	-	W
P_{load}	Operational power		-	7	-	W
P_{VBAT}	Vbat power		-	7	-	W
$P_{3.3V}$	3.3V power		-	1	-	W

NOTE

The figures in Table 6 greatly depend on the end application.

4. Pinout

Table 7. Pinout for the Raspberry Pi Compute Module 4 SODIMM

Pin	Signal	Description
1	GND	Ground (0V)
2	EMMC_DISABLE_N	Drive low to force USB boot. Internal 10kΩ pull up to 3.3V must be driven by an open collector signal.
3	GPIO0	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
4	SDX_VDD	SD card/eMMC IO supply: typically +3.3V, but can be 1.8V if external eMMC supports 1.8V signalling.
5	GPIO1	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
6	SDX_VDD	SD card/eMMC IO supply: typically +3.3V, but can be made 1.8V if external eMMC supports 1.8V signalling.
7	GND	Ground (0V)
8	GND	Ground (0V)
9	GPIO2	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
10	SDX_CLK	SD card/eMMC clock signal (only available on CM4SLite).
11	GPIO3	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
12	SDX_CMD	SD card/eMMC command signal (only available on CM4SLite).
13	GND	Ground (0V)
14	GND	Ground (0V)
15	GPIO4	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
16	SDX_D0	SD card/eMMC Data0 signal (only available on CM4SLite).
17	GPIO5	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
18	SDX_D1	SD card/eMMC Data1 signal (only available on CM4SLite).
19	GND	Ground (0V)
20	GND	Ground (0V)
21	GPIO6	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
22	SDX_D2	SD card/eMMC Data2 signal (only available on CM4SLite).
23	GPIO7	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
24	SDX_D3	SD card/eMMC Data3 signal (only available on CM4SLite).
25	GND	Ground (0V)
26	GND	Ground (0V)
27	GPIO8	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
28	GPIO28	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
29	GPIO9	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
30	GPIO29	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.

31	GND	Ground (0V)
32	GND	Ground (0V)
33	GPIO10	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
34	GPIO30	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
35	GPIO11	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
36	GPIO31	GPIO: typically a 3.3V signal, but can be a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
37	GND	Ground (0V)
38	EEPROM_nWP	Leave floating. Internally pulled up to `GPIO28-45_VDD` via 100kΩ (V_{IL} < 0.8V), but can be grounded to prevent writing to the on-board EEPROM, which stores the bootcode.
39	GPIO0-27_VDD	GPIO0-27 VDD: typically a 3.3V for 3.3V signalling, but can be a 1.8V for 1.8V signalling.
40	GPIO0-27_VDD	GPIO0-27 VDD: typically a 3.3V for 3.3V signalling, but can be a 1.8V for 1.8V signalling.
41	GPIO28-45_VDD	GPIO28-45 VDD: typically a 3.3V for 3.3V signalling, but can be a 1.8V for 1.8V signalling.
42	GPIO28-45_VDD	GPIO28-45 VDD: typically a 3.3V for 3.3V signalling, but can be a 1.8V for 1.8V signalling.
43	GND	Ground (0V)
44	GND	Ground (0V)
45	GPIO12	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
46	GPIO32	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
47	GPIO13	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
48	GPIO33	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
49	GND	Ground (0V)
50	GND	Ground (0V)
51	GPIO14	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
52	GPIO34	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
53	GPIO15	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
54	GPIO35	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
55	GND	Ground (0V)
56	GND	Ground (0V)
57	GPIO16	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
58	GPIO36	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
59	GPIO17	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
60	GPIO37	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
61	GND	Ground (0V)
62	GND	Ground (0V)
63	GPIO18	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
64	GPIO38	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
65	GPIO19	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.

66	GPIO39	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
67	GND	Ground (0V)
68	GND	Ground (0V)
69	GPIO20	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
70	GPIO40	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
71	GPIO21	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
72	GPIO41	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
73	GND	Ground (0V)
74	GND	Ground (0V)
75	GPIO22	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
76	GPIO42	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
77	GPIO23	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
78	GPIO43	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
79	GND	Ground (0V)
80	GND	Ground (0V)
81	GPIO24	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
82	GPIO44	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
83	GPIO25	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
84	GPIO45	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO28-45_VDD to 1.8V.
85	GND	Ground (0V)
86	GND	Ground (0V)
87	GPIO26	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
88	HDMI_HPD_N_1V8	Input HDMI hot plug. Internally pulled up to +1.8V via a 2.2kΩ resistor.
89	GPIO27	GPIO: typically a 3.3V signal, but can be made a 1.8V signal by connecting GPIO0-27_VDD to 1.8V.
90	EMMC_EN_N_1v8	Internal 2.2kΩ pullup to 1.8V.
91	GND	Ground (0V)
92	GND	Ground (0V)
93	DSI0_DN1	Output Display0 D1 negative
94	DSI1_DP0	Output Display1 D0 positive
95	DSI0_DP1	Output Display0 D1 positive
96	DSI1_DN0	Output Display1 D0 negative
97	GND	Ground (0V)
98	GND	Ground (0V)
99	DSI0_DN0	Output Display0 D0 negative
100	DSI1_CP	Output Display1 clock positive
101	DSI0_DP0	Output Display0 D0 positive

102	DSI1_CN	Output Display1 clock negative
103	GND	Ground (0V)
104	GND	Ground (0V)
105	DSI0_CN	Output Display0 clock negative
106	DSI1_DP3	Output Display1 D3 positive
107	DSI0_CP	Output Display0 clock positive
108	DSI1_DN3	Output Display1 D3 negative
109	GND	Ground (0V)
110	GND	Ground (0V)
111	HDMI_CLK_N	Output HDMI clock negative
112	DSI1_DP2	Output Display1 D2 positive
113	HDMI_CLK_P	Output HDMI clock positive
114	DSI1_DN2	Output Display1 D2 negative
115	GND	Ground (0V)
116	GND	Ground (0V)
117	HDMI_D0_N	Output HDMI TX0 negative
118	DSI1_DP1	Output Display1 D1 positive
119	HDMI_D0_P	Output HDMI TX0 positive
120	DSI1_DN1	Output Display1 D1 negative
121	GND	Ground (0V)
122	GND	Ground (0V)
123	HDMI_D1_N	Output HDMI TX1 negative
124	Not connected	
125	HDMI_D1_P	Output HDMI TX1 positive
126	Not connected	
127	GND	Ground (0V)
128	GND	Ground (0V)
129	HDMI_D2_N	Output HDMI TX2 negative
130	Not connected	
131	HDMI_D2_P	Output HDMI TX2 positive
132	Not connected	
133	GND	Ground (0V)
134	GND	Ground (0V)
135	CAM1_DP3	Input Camera1 D3 positive
136	CAM0_DP0	Input Camera0 D0 positive
137	CAM1_DN3	Input Camera1 D3 negative

138	CAM0_DN0	Input Camera0 D0 negative
139	GND	Ground (0V)
140	GND	Ground (0V)
141	CAM1_DP2	Input Camera1 D2 positive
142	CAM0_CP	Input Camera0 clock positive
143	CAM1_DN2	Input Camera1 D2 negative
144	CAM0_CN	Input Camera0 clock negative
145	GND	Ground (0V)
146	GND	Ground (0V)
147	CAM1_CP	Input Camera1 clock positive
148	CAM0_DP1	Input Camera0 D1 positive
149	CAM1_CN	Input Camera1 clock negative
150	CAM0_DN1	Input Camera0 D1 negative
151	GND	Ground (0V)
152	GND	Ground (0V)
153	CAM1_DP1	Input Camera1 D1 positive
154	Not Connected	
155	CAM1_DN1	Input Camera1 D1 negative
156	Not Connected	
157	GND	Ground (0V)
158	GND	Ground (0V)
159	CAM1_DP0	Input Camera1 D0 positive
160	Not Connected	
161	CAM1_DN0	Input Camera1 D0 negative
162	Not Connected	
163	GND	Ground (0V)
164	GND	Ground (0V)
165	USB_DP	USB D+
166	TVDAC	Video DAC output (TV out)
167	USB_DM	USB D-
168	USB_OTGID	Input (3.3V signal) USB OTG Pin. Internally pulled up. When grounded the CM4S becomes a USB host, but the correct OS driver also needs to be used.
169	GND	Ground (0V)
170	GND	Ground (0V)
171	HDMI_CEC	Input HDMI CEC: internally pulled up with a 27kΩ to +3.3V.
172	VC_TRST_N	VideoCore nTRST pin, usually left unconnected

173	HDMI_SDA	Bidirectional HDMI SDA 5V-tolerant, requires a pullup as per HDMI specification.
174	VC_TDI	VideoCore TDI pin, usually left unconnected
175	HDMI_SCL	Bidirectional HDMI SCL 5V-tolerant, requires a pullup as per HDMI specification.
176	VC_TMS	VideoCore TMS pin, usually left unconnected.
177	RUN	Bidirectional pin. Can be driven low to reset the CM4S CPU. As an output, a high signals that power is good and CPU is running. Internally pulled up to +3.3V via 10kΩ, but clamped to VBAT via a diode if VBAT is lower than +3.3V.
178	VC_TDO	VideoCore TDO pin, usually left unconnected.
179	VDD_CORE	Do not connect anything to this pin.
180	VC_TCK	VideoCore TCK pin, usually left unconnected.
181	GND	Ground (0V)
182	GND	Ground (0V)
183	Not Connected	Can either be unconnected or +1.8V.
184	Not Connected	Can either be unconnected or +1.8V.
185	Not Connected	Can either be unconnected or +1.8V.
186	Not Connected	Can either be unconnected or +1.8V.
187	GND	Ground (0V)
188	GND	Ground (0V)
189	VDAC	VDD for TV out
190	VDAC	VDD for TV out
191	+3.3V	+3.3V power input
192	+3.3V	+3.3V power input
193	+3.3V	+3.3V power input
194	+3.3V	+3.3V power input
195	GND	Ground (0V)
196	GND	Ground (0V)
197	VBAT	+2.5V to +5V power input
198	VBAT	+2.5V to +5V power input
199	VBAT	+2.5V to +5V power input
200	VBAT	+2.5V to +5V power input

All ground pins should be connected.

The voltage on GPIO pins 0-45 must not exceed `+3.3V` if +3.3V signalling is used or `+1.8V` if +1.8V signalling is used.

4.1. Differential pairs

It is recommended that P/N signals within a pair are matched to better than 0.15mm. Often, matching between pairs is not so critical: e.g. HDMI pair-to-pair matching should be better than 25mm, so on a typical board no extra matching is required.

4.1.1. 100Ω differential pair signal lengths

On the CM4S all differential pairs are matched to better than 0.05mm (P/N signals).

NOTE

It is recommended that pairs are also matched on the interface board.

On the CM4S, pair-to-pairs are not always matched, as many interfaces do not require very accurate matching between pairs. Table 8 documents the CM4S track-length difference within each group. (A non-zero value represents how much longer in mm that track is, when compared to the signal with zero length difference.)

Table 8. 100Ω differential pair signal lengths

Signal	Length
CAM0_C_N	3.09
CAM0_C_P	3.09
CAM0_D0_N	0
CAM0_D0_P	0
CAM0_D1_N	2.97
CAM0_D1_P	3.00
CAM1_C_N	3.71
CAM1_C_P	3.76
CAM1_D0_N	2.57
CAM1_D0_P	2.53
CAM1_D1_N	1.97
CAM1_D1_P	1.96
CAM1_D2_N	0.03
CAM1_D2_P	0
CAM1_D3_N	0.38
CAM1_D3_P	0.34
DSI0_C_N	0.94
DSI0_C_P	0.98
DSI0_D0_N	0
DSI0_D0_P	0.01
DSI0_D1_N	0.27
DSI0_D1_P	0.29
DSI1_C_N	2.82
DSI1_C_P	2.82
DSI1_D0_N	0
DSI1_D0_P	0.01

DSI1_D1_N	2.09
DSI1_D1_P	2.08
DSI1_D2_N	4.15
DSI1_D2_P	4.16
DSI1_D3_N	4.08
DSI1_D3_P	4.09
HDMI_CLK_N	0.04
HDMI_CLK_P	0
HDMI_TX0_N	0.02
HDMI_TX0_P	0.04
HDMI_TX1_N	0.23
HDMI_TX1_P	0.23
HDMI_TX2_N	0.41
HDMI_TX2_P	0.36

4.1.2. 90Ω differential pair signal lengths

On the CM4S all differential pairs are matched to better than 0.05mm (P/N signals).

NOTE

It is recommended that pairs are also matched on the interface board.

Pair-to-pairs aren't always matched as many interfaces don't require very accurate matching between pairs. Table 9 documents the CM4S track-length difference within each group. (A non-zero value represents how much longer in mm that track is, when compared to the signal with zero length difference.)

Table 9. 90Ω differential pair signal lengths

Signal	Length
USB2_P	0.03
USB2_N	0

5. Power

5.1. Power-up sequencing

The CM4S requires a VBAT (2.5V to 5V) and +3.3V supplies. Older Compute Modules required +1.8V as well; +1.8V is no longer used, but can be supplied for backward compatibility.

If the EEPROM is to be write-protected, then the `EEPROM_nWP` should be low before power-up.

If the CM4S is to be booted using USB, then `EMMC_DISABLE_N` needs to be low within 1µs of +3.3V rising.

The power-up sequence will start when +3.3V rail is above +3V. The order of events is as follows:

1. If VBAT is going to be greater than +3.3V, VBAT should rise first
2. +3.3V rises
3. VBAT rises if it is lower than +3.3V
4. `RUN` rises at least 10µs after the last rail to power-up.

5.2. Power-down sequencing

The operating system should be shut down before the power is removed, to ensure that the file system remains consistent. If this can't be achieved, then a filesystem like `btrfs`, `f2fs` or `overlayfs` (use `raspi-config` to enable this) should be considered.

Once the operating system has shut down, the PSU rails may be removed in the reverse order of power-up: i.e. the lowest voltage rail is removed first. Taking the RUN pin low will reset the BCM2711.

5.3. Power consumption

The exact power consumption of the CM4S will greatly depend on the tasks being run on the CM4S. Idle power consumption is typically 1.5W, but this varies considerably depending on the operating system. Operating power consumption is typically around 7W; again, this greatly depends on the operating system and the tasks being executed.

Appendix A: Troubleshooting

The CM4S has a number of stages of power-up before the CPU starts. If there is an error at any of the stages, power-up will be halted.

Bootloader

1. Connect a HDMI cable to see if the HDMI diagnostics screen appears.
2. Connect a USB serial cable to GPIO pins 14 and 15.
    a. See https://www.raspberrypi.com/documentation/computers/configuration.html#configuring-uarts for details.
3. Short the `EMMC_DISABLE_N` pin to ground to force USB boot mode.
    a. See https://www.raspberrypi.com/documentation/computers/compute-module.html#flashing-the-compute-module-emmc

rpi-eeprom-update

1. CM4S will not run `recovery.bin` from from the EMMC (or SD Card on CM4SLite). Therefore, the only way to update the bootloader EEPROM is via `usbboot` or self-update.

EEPROM write-protect

The on-board EEPROM can be write-protected by shorting `EEPROM_nWP` to ground.

1. See https://www.raspberrypi.com/documentation/computers/raspberry-pi.html#raspberry-pi-4-bootloader-configuration

Firmware

1. A 5.4 or newer kernel and the latest firmware release is required. These can be updated by using usbboot to mount the EMMC as a USB MSD device.
2. Nightly OS images are now available which contain `rpi-update` master firmware + kernel. Bug fixes for CM4S will normally be provided via these images except where a test/patch binary is required.
    a. See http://downloads.raspberrypi.org/nightlies/

Kernel

1. The updated OS images use the new Raspberry Pi Compute Module 4 SODIMM device tree file. If that is not found then the Raspberry Pi 4 Model B device tree file will be used.
    a. See https://github.com/raspberrypi/linux/blob/rpi-5.4.y/arch/arm/boot/dts/bcm2711-rpi-cm4.dts

Appendix B: Availability

Support

For documentation please see the Compute Module Hardware documentation section of the Raspberry Pi website. Support questions can be posted to the Raspberry Pi forum.

Ordering codes

Table 10. Part number options

Model	RAM LPDDR4	eMMC Storage
CM4S	01 = 1GB	000 = 0GB (Lite)
	02 = 2GB	008 = 8GB
	04 = 4GB	016 = 16GB
	08 = 8GB	032 = 32GB
Example Part Number		
CM4S	01	032

Table 11. Ordering options

RAM LPDDR4	Storage eMMC	RPL #	Part Number	MOQ	RRP
1GB	OGB (Lite)	SC0762	CM4S01000	200	$ 25.00
1GB	8GB	SC0763	CM4S01008	200	$ 30.00
1GB	16GB	SC0764	CM4S01016	200	$ 35.00
1GB	32GB	SC0765	CM4S01032	200	$ 40.00
2GB	0GB (Lite)	SC01762	CM4S02000	200	$ 30.00
2GB	8GB	SC01763	CM4S02008	200	$ 35.00
2GB	16GB	SC01764	CM4S02016	1000	$ 40.00
2GB	32GB	SC01765	CM4S02032	200	$ 45.00
4GB	0GB (Lite)	SC01766	CM4S04000	200	$ 40.00
4GB	8GB	SC01767	CM4S04008	1000	$ 45.00
4GB	16GB	SC01768	CM4S04016	1000	$ 50.00
4GB	32GB	SC01769	CM4S04032	200	$ 55.00
8GB	0GB (Lite)	SC01770	CM4S08000	1000	$ 60.00
8GB	8GB	SC01771	CM4S08008	1000	$ 65.00
8GB	16GB	SC01772	CM4S08016	1000	$ 70.00
8GB	32GB	SC01773	CM4S08032	200	$ 75.00

NOTE

RRP was correct at time of publication and excludes taxes.

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